

FIGURE 1

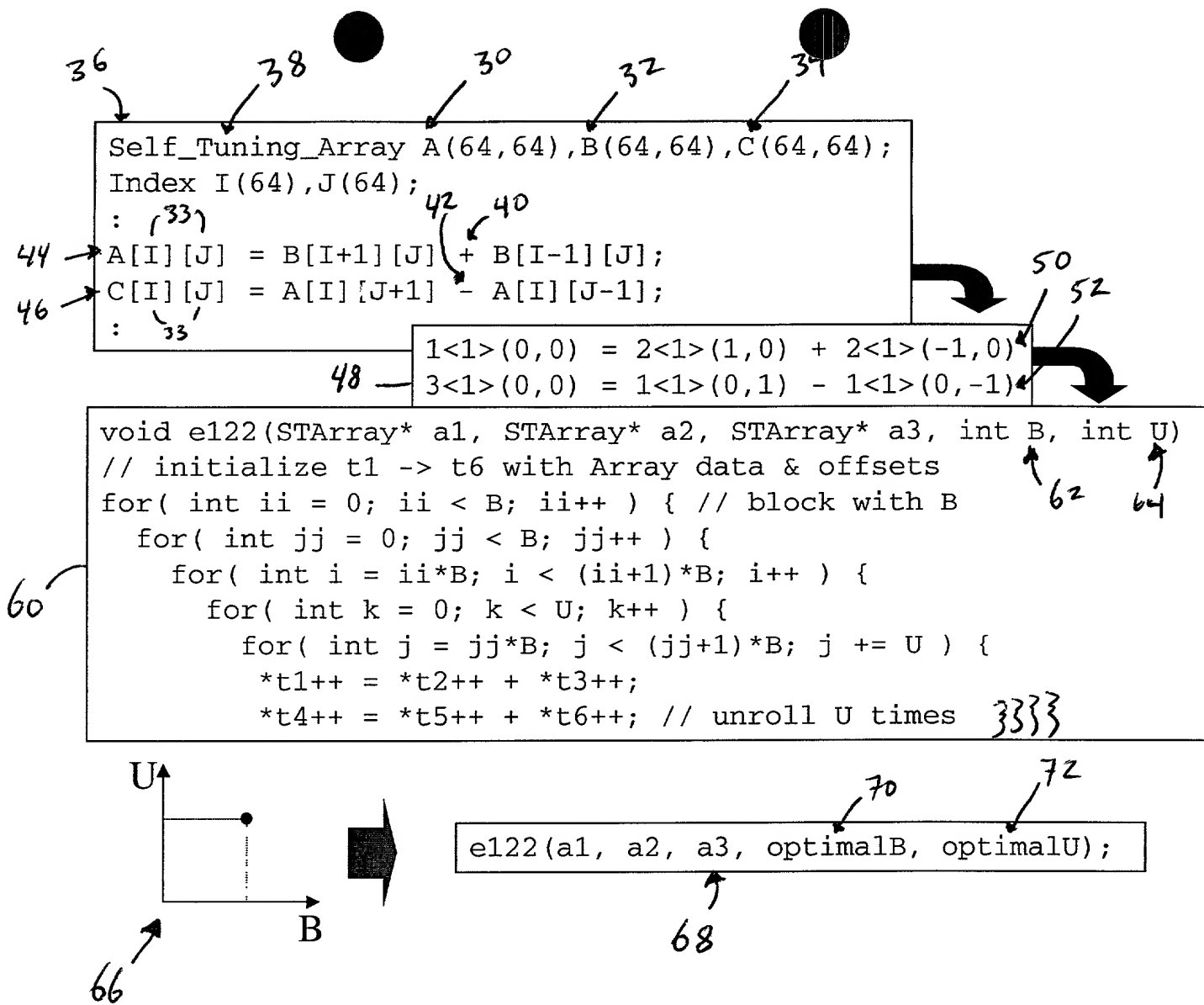


FIGURE 2

FIG. 3 is a block diagram of a system for processing data in accordance with the present invention. The system includes a processor 100, a memory 102, and a data source 104. The processor 100 is connected to the memory 102 and the data source 104. The processor 100 is configured to receive data from the data source 104 and store it in the memory 102. The processor 100 is also configured to retrieve data from the memory 102 and process it. The processor 100 is further configured to output the processed data to the data source 104. The system is designed to efficiently process large amounts of data by utilizing the memory 102 to store intermediate results and the processor 100 to perform the necessary calculations.

# User Code 100

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104 {
: A[I][J] = B[I+1][J] + B[I-1][J];
: C[I][J] = A[I][J+1] - A[I][J-1];
: D[I][J] = C[I+1][J] + C[I-1][J];
: E[I][J] = D[I][J+1] - D[I][J-1];
:
:
:
109 {
: A[I][J] = B[I][J] + D[I][J];
: C[I][J] = B[I][J] - D[I][J];
:
:
:
113 {
: A[I][J] = C[I-1][J] + B[I-1][J+1];
: B[I][J] = C[I][J+1] - B[I][J+1];
:
:

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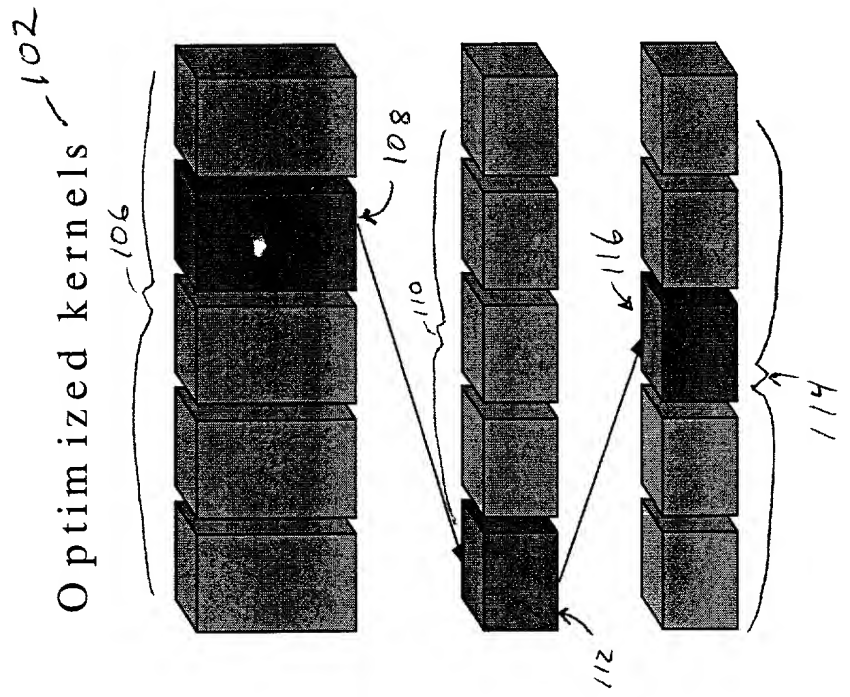


FIGURE 3